Architecture and Algorithm For High Precision Image Rejection and Spurious Rejection Mixers Using Digital Compensation

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Abstract - **A high precision IRM and SRM architecture composed of analog RF and digital IF mixers are proposed. A precise and fast measurement algorithm for gain and phase mismatches is proposed, which are, then, compensated by digital signal processing. A prototype 2.4GHz IRM with IRR>70 and BW=11MHz is demonstrated by using this technique.**

I. INTRODUCTION

For single chip integration, all filters in transceiver must be eliminated, which are image rejection filter in receiver and spurious rejection filter in transmitter. it is well known that these filtes can indeed be eliminated by using mixers, which are called as the image rejection mixer (IRM) in the receiver and spurious rejection mixer (SRM) in the transmitter, respectively.

There are two types of IRM's. One is the Hartley architecture and the other is the Weaver architecture.[1] The Weaver architecture consists of more than 4 mixers, but the image rejection bandwidth of the Weaver architecture is wider than that of the Hartley architecture. The limitation of image rejection in the Weaver architecture comes from the phase mismatch of quadrature LO phase shifter and the gain mismatch between the mixers. Due to the mismatches in the RF circuits, however, it is not easy to obtain over 30dB image rejection by using only circuit design and layout technique. Recently, we have shown that more than 80dB IR can be obtained at single frequency using digital compensation.[2]

In this paper, we extend our previous work[2] to signals with finite bandwidth as well as to SRM in transmitter.

II. NEW ARCHITECTURE AND ALGORITHM FOR IMAGE REJECTION

The proposed IRM architecture is shown in Figure 1.[2] The unwanted mismatches generated in analog domain are estimated in mismatch estimation block by sweeping the mismatch estimation variables in the digital domain.

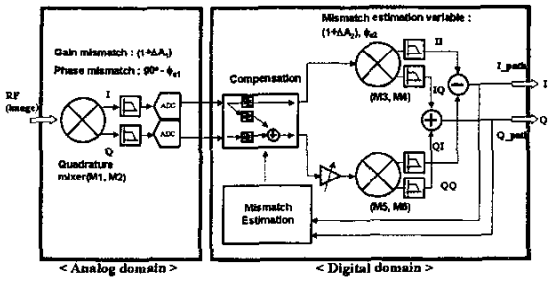

Figure 1. The proposed weaver architecture with the compensation block of the phase mismatch and the gain mismatch. [ΔA_1=gain mismatch between M_1 and M_2, $\phi_{\varepsilon 1}$=phase mismatch of 1st LO, ΔA_2=gain estimation variable between M_3 and M_5 (or between M_4 and M_6), $\phi_{\varepsilon 2}$=phase estimation variable of 2nd LO]

After this, the filter coefficients in the compensation block are calculated from this estimated mismatch.

Firstly, we repeat the mismatch measurement introduced in ref. [2]. Let us assume that the phase difference between mixer M3 and M4 is set by $90°+\phi_{\varepsilon 2}$ and the phase difference between mixer M5 and M6 is set by $90°-\phi_{\varepsilon 2}$, the signal expression in each output node, then, is shown as follows.

$$II(t)=\frac{(1+\Delta A_1)}{4}\cos(\Delta\omega)t,\quad IQ_m(t)=\frac{(1+\Delta A_1)}{4}\sin(\Delta\omega t+\phi_{\varepsilon 2})$$

$$QI(t)=-\frac{(1+\Delta A_2)}{4}\sin(\Delta\omega+\phi_{\varepsilon 1})t,\quad QQ(t)=\frac{(1+\Delta A_2)}{4}\cos(\Delta\omega t+\phi_{\varepsilon 1}-\phi_{\varepsilon 2}) \quad (1)$$

Then the gain and phase mismatch can be measured as follows.

$$(II-QQ)^2(t)+(IQ_m+QI)^2(t)\cong$$

$$\frac{1}{16}\left[(\Delta A_1-\Delta A_2)\cos(\Delta\omega)t+(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})\sin(\Delta\omega)t\right]^2$$

$$+\frac{1}{16}\left[(\Delta A_1-\Delta A_2)\sin(\Delta\omega)t-(\phi_{\varepsilon 1}-\phi_{\varepsilon 2})\cos(\Delta\omega)t\right]^2$$

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$$= \frac{1}{16}\left[(\Delta A_1 - \Delta A_2)^2 + (\phi_{\varepsilon 1} - \phi_{\varepsilon 2})^2\right] \quad ..(2)$$

Where $\Delta A_1, \Delta A_2, (\Delta A_1 - \Delta A_2) << 1, \sin(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}) \cong \phi_{\varepsilon 1} - \phi_{\varepsilon 2}$, $\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}) \cong 1$

Note that equation (2) has very interesting properties that the gain and phase mismatches are decoupled and convex, which allows us to measure them, independently and uniquely. In ref. [2], we applied at single image frequency. We now extend above work to signals with finite bandwidth, where the phase and gain mismatches aren't constant over the given bandwidth. So, the frequency dependant mismatch variation must be compensated at multiple frequencies as shown in Figure 2. Here α_i's and β_i's are determined, so as to minimize the mismatches measured at several frequencies in the interested bandwidth.

III. APPLICATION OF DIGITAL COMPENSATION TO SRM

Now let us apply our proposed IRM method to SRM. Our proposed SRM architecture is shown in Figure 3. The quadrature up-converted signals have the unwanted spurious frequency (LO+IF) due to the mismatches. These mismatches might come from non-ideal quadrature LO, no perfect match between mixers, and so forth. The unwanted frequency (LO+IF) should be rejected and the wanted frequency (LO-IF) should be maximized.

To estimate the mismatches in SRM, we down convert only the spurious component in the receiver block. The spurious component at high frequency is down converted into low frequency in digital domain for easily estimating mismatch. Note that the quadrature signal in the transmitter including mismatch is down-converted by a single mixer in the receiver. If quadrature mixers are used, the additional mismatch between quadrature signals would be added.

For all frequencies in the BW, the mismatches between quadrature signals are measured in the estimation block. After this, the filter coefficient of compensation block is calculated by this measured mismatch. The final SRM architecture is shown in Figure 3.

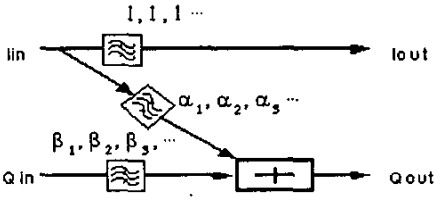

Figure 2. Mismatch compensation method

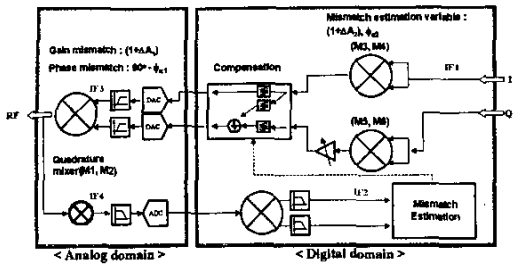

Figure 3. The proposed spurious rejection architecture with the compensation block of the phase mismatch and the gain mismatch.[ΔA_1=gain mismatch between M_1 and M_2, $\phi_{\varepsilon 1}$=phase mismatch of 1st LO(M1, M2), ΔA_2=gain estimation variable between M_3 and M_5 (or between M_4 and M_6), $\phi_{\varepsilon 2}$=phase estimation variable of 2nd LO(M3, M4, M5, M6)]

Now let's explain how to measure mismatches in SRM. If we assume baseband signal is ideal, we obtain the following signals at node I and Q, respectively.

$$I(t) = \cos(\omega_{IF1} t), \quad Q(t) = \sin(\omega_{IF1} t) \quad .....(3)$$

If we let the phase difference between mixer M3 and M4 be set by $90°-\phi_{\varepsilon 2}$ and the phase difference between mixer M5 and M6 by $90°-\phi_{\varepsilon 2}$, the signal expression in estimation block by the quadrature input signal at IF2 node is shown as follows.

$$IF2\_I^2 + IF2\_Q^2$$
$$= \frac{1}{16^2}\left[(\Delta A_1 - \Delta A_2)^2 + (\phi_{\varepsilon 1} - \phi_{\varepsilon 2})^2\right] \quad .....(4)$$

Where $\Delta A_1, \Delta A_2, (\Delta A_1 - \Delta A_2) << 1, \sin(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}) \cong \phi_{\varepsilon 1} - \phi_{\varepsilon 2}$, $\cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}) \cong 1$

In equation (4), note that the high frequency mismatches in SRM architecture can be exactly measured as was done in IRM architecture. Because the global minimum equation is conformed, the gain and the phase mismatch are estimated, independently and uniquely. We can find that the only one value can make equation (4) minimum. After mismatch estimation, the compensation block from estimated mismatches should be revised like as IRM architecture.

In the SRM architecture, the receiver block in Figure 3 needed for only estimating mismatches is not an additional burden, because the part of receiver in transceiver can be reused.[6]

IV. APPLICATION OF PROPOSED COMPENSATION METHOD TO PROTOTYPE IRM WITH FINITE BANDWIDTH

The proto-type 2400MHz image rejection mixer is implemented as shown in Figure 4. The fixed LO frequency is 2400MHz and the frequency range of RF image band is 2387.5 ~ 2398.75MHz.

The image carrier is multiplied by in-phase and quadrature phase LO and converted down to IF1 in-phase (I) signal and quadrature phase (Q) signal at the 1st IF stage. The packaged passive mixers are used for the 1st mixers (M_1 and M_2) in Figure 1 and 4. The 90° phase shifter for 2400MHz quadrature LO generation is implemented with the branch-line coupler. The power of RF signal is divided by the Wilkinson power divider. The amplifier is placed at IF1 node for satisfying the full input range of ADC in Figure 1.

The image signal is down-converted into the quadrature phase IF1 and then, the IF1 frequency is over-sampled by 4 ~ 100 times in 12bits ADC. Because our architecture is limited by SFDR of ADC, the bits of ADC is increased into 12bits for obtaining more than 80dB IRR[6]. The sampling clock of ADC is fixed to 50MHz, whereas the IF1 frequency, which is signal down-converted from image frequency at RF node, is varied in 1.25 ~ 12.5MHz.

The digital domain signal processing in Figure 1 is done by computer simulation using Matlab. The sampled 24000 points are used for the input of Matlab simulation. At each image frequency, the estimated mismatch is plotted in Figure 5 and Figure 6.

The gains (α, β) of filters in compensation block in Figure 1 are calculated by using the estimated mismatch ($\phi_{\varepsilon 2}$, ΔA_2) in Figure 5 and Figure 6.

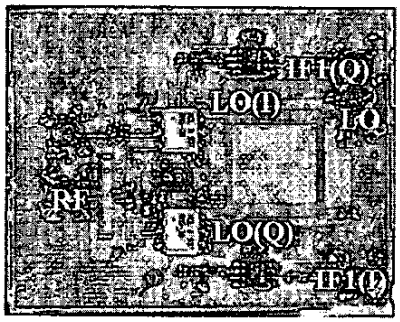

Figure 4. Quadrature down-converter: LO part(branch line coupler), RF(Wilkinson power divider), mixer(M1, M2), IF amplifier.

In Table 1, The FIR filter is designed by the calculated gain of filters according to discrete frequency and designed by automatic fitting offered in Matlab simulator. In Figure 7, the IRR characteristic is plotted when we include mismatch compensation block. The number of tap in filter make an effect on exactness in fitting of coefficients. So, the case using 1000 taps FIR filter shows the best performance, 80dB image rejection ratio in 11MHz BW. The case using 100 taps FIR filter shows more than 70dB image rejection ratio with a little degradation. Using more than 100 taps in designing filters is impossible to implement. Therefore, we can conclude the latter case is the limitation of our architecture.

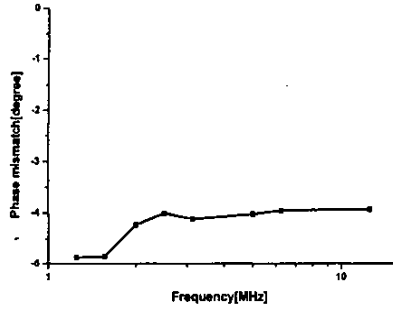

Figure 5. Phase mismatch estimation variable ($\phi_{\varepsilon 2}$): measured phase mismatch.

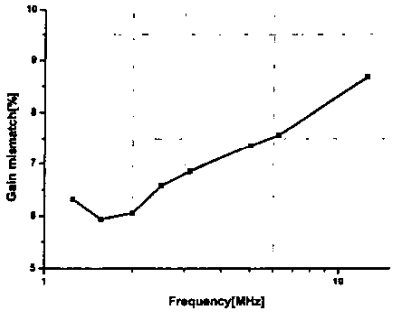

Figure 6. Gain mismatch estimation variable (ΔA_2): measured gain mismatch.

Table 1. α and β (calculated), α and β (passband gain of filter) [dB] : The filters are designed by 1000 tap FIR.

freq.[MHz]	β(calcu.)	β(filter)	α(calcu.)	α(filter)
1.25	-0.53689	-0.53672	-21.40886	-21.40507
1.56	-0.5013	-0.50172	-21.44936	-21.4499
2	-0.51922	-0.5193	-22.61984	-22.61184
2.5	-0.56969	-0.56921	-23.09624	-23.08857
3.125	-0.5944	-0.59464	-22.85481	-22.86174
5	-0.64298	-0.643	-23.04742	-23.05127
6.25	-0.66298	-0.66266	-23.1947	-23.18842
12.5	-0.76855	-0.76862	-23.24435	-23.24644

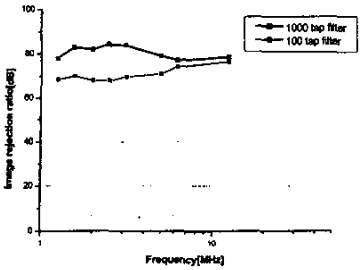

Figure 7. IRR characteristics of proposed IRM architecture after mismatch compensation.[6]

V. CONCLUSIONS AND DISCUSSION

In this paper, we proposed new image IRM and SRM architecture. We derived the simple global minimum equation according to the mismatch estimation variable for the two architectures. In two architectures, the new compensation method modified from conventional narrow compensation method for considering mismatch variation in BW is proposed and verified by applying to the prototype 2400MHz IRM architecture. In case of IRM architecture, the total architecture including the mismatch compensation block realized by the digital signal processing causes to exhibit so much high image rejection in Figure 7. The compared IRR characteristic with the published architecture is shown in Figure 8. Because the specification of image rejection and spurious rejection at the receiver and transmitter is around 70 ~ 80dB, we think that our architectures can be replace with expensive SAW filters.

We proposed the architectures in which the expensive SAW filters are removed and suggested the future transceiver architecture for single chip architecture.

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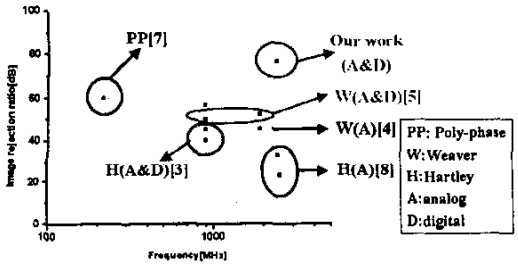

Figure 8. Maximum IRR characteristic in BW of the published conventional architecture.[6]

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